



Hot SWAP

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Hot Swap Circuit Gets InfiniBand Power Onto Your Module

An InfiniBand™ backplane distributes bulk power at 12V DC to a number of plug-in modules, each having a DC/DC converter that steps the 12V supply down to the voltages required locally. A pass transistor on each module isolates the converter's input

capacitors during module plug-in, allowing modules to be added without disturbing others on the backplane. The requirements governing module hardware design are found in the InfiniBand Architecture Specification, Volume 2, Release 1.0.

Figure 1 shows the circuit. Pow-

er is supplied from the backplane at 12V DC between VB_In and VB_Ret. There are two control signals, VBxEn_L (active low) and Local Power Enable (active high). The LTC1642 Hot Swap™ controller IC performs four functions in this circuit. It controls pass transistor Q1's gate in re-

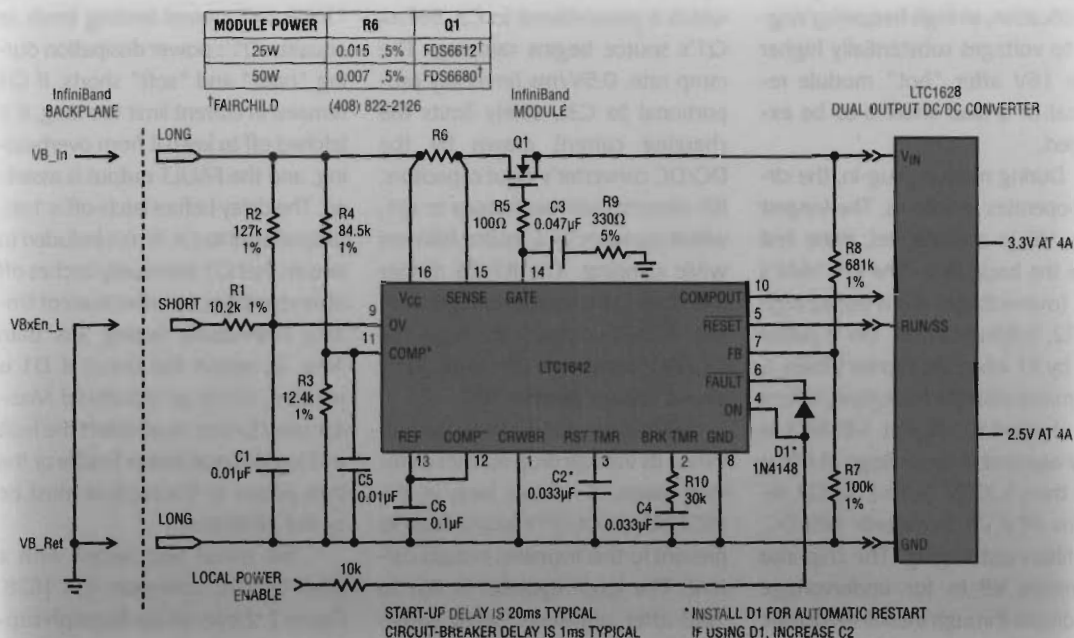


FIGURE 1. LTC1642 INFINIBAND HOT SWAP CIRCUIT

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sponse to both signals; it limits Q1's drain current; it monitors VB_In for both overvoltage and undervoltage conditions; and starts the DC/DC converter downstream. The LTC1642 was selected because it can respond to two control inputs and because its voltage range suits the application's requirements. Although the backplane supplies 12V nominally, the InfiniBand specification requires steady-state operation to 14V DC and up to 16V for 1ms transients; this is satisfactory because the LTC1642 is fully specified for operation up to 16.5V. Its 33V maximum rating is an added benefit: capacitive bypassing at VB_In is limited to 5nF by the specification, so high frequency ringing to voltages substantially higher than 16V after "hot" module removal or a load short is to be expected.

During module plug-in, the circuit operates as follows. The longest pins, VB_In and VB_Ret, mate first with the backplane. The LTC1642's OV (overvoltage) pin is pulled high by R2, holding Q1 off. OV is pulled low by R1 when the shorter VBxEn_L pin mates with the backplane, where it is shorted to VB_Ret. VBxEn_L is only asserted if the voltage at OV is less than 1.223V ($\pm 1\%$), so Q1 remains off if VB_In exceeds 16V DC; C1 filters out ringing. The chip also monitors VB_In for undervoltage conditions through the R3-R4 divider, holding the COMPOUT pin low when VB_In is less than 10V. COMPOUT can be tied to the ON pin to lock out undervoltages on VB_In. Local Power Enable is driven by an

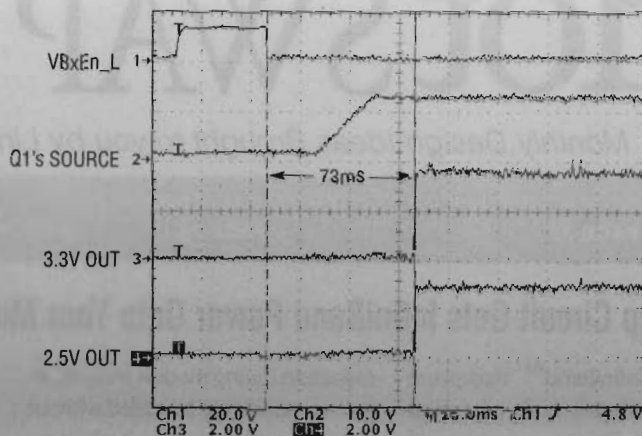


FIGURE 2. WAVE FORMS DURING INFINIBAND MODULE PLUG IN

InfiniBand Management Device, powered separately from a 5V auxiliary. After assertion of both control signals, there is a delay of 20ms, which is proportional to C2, before Q1's source begins ramping. The ramp rate, 0.5V/ms (inversely proportional to C3), safely limits the charging current drawn by the DC/DC converter's input capacitors. R5 prevents self-oscillations in Q1, which operates as a source follower while ramping. The R7-R8 divider monitors Q1's source voltage, with the RESET output holding the DC/DC converter off until Q1's source voltage reaches 10V.

R6 senses Q1's drain current. When its voltage drop reaches a limiting value, a control loop in the LTC1642 servos Q1's gate voltage to prevent further increases in drain current. The loop regulates in 5 μ s to 10 μ s after activation, safely within the 20 μ s specification. R9 works with C3 to compensate this loop. Q1's maximum allowed drain current increases as its source voltage, sensed by the R7-R8 divider, increases. The

voltage across R6 is limited to 23mV when the LTC1642's FB pin is grounded, increasing gradually to 53mV when FB is 1V or more. This "foldback" current limiting tends to equalize Q1's power dissipation during "hard" and "soft" shorts. If Q1 remains in current limit too long, it is latched off to keep it from overheating, and the FAULT output is asserted. The delay before latch-off is 1ms, proportional to C4. R10 is included to ensure that Q1 eventually latches off after repetitive, transient current limiting individually lasting less than 1ms. To restart the circuit if D1 is omitted, either an InfiniBand Management Device must detect the fault and toggle Local Power Enable or the bulk power to the module must be cycled off then on.

The circuit was tested with a 50W DC/DC converter, LTC1628. Figure 2 shows an oscillograph captured during module plug-in. The delay from VBxEn_L assertion to the converter's output coming into regulation is 73ms, safely within the 500ms InfiniBand specification. ■



2-Wire Bus Buffer Allows I²C™ or SMBus to be Hot Swapped and Extended

Linear Technology introduces the LTC4300, a bi-directional bus buffer that allows cards with 2-wire interfaces to be inserted or removed under power without corrupting the signals. It acts as a repeater by buffering the capacitance of additional components connected to the bus. Control circuitry prevents the backplane signals from being connected to the card until the bus is idle or a stop bit occurs and a 1V pre-charge reduces disruption on the bus when the circuits are connected.

The LTC4300 simplifies the task of using a 2-wire bus to manage a large number of cards in network server, desktop PC or telecom environment.

With a 2-wire bus such as I²C™ or SMBus, each added component on the bus adds capacitance that slows the rise time of the signals. Adding stronger pull-up resistors makes it difficult to meet the low logic level voltage requirement. Hot swapping a card is even more difficult because these added components corrupt the data when connected or removed.

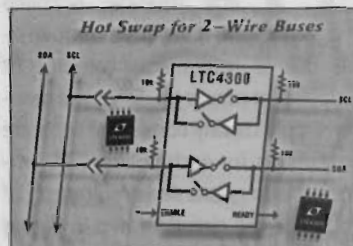


FIGURE 1. BUS BUFFER ALLOWS I²C CARDS TO BE HOT SWAPPED

Summary of Features:

- Bi-Directional Buffer for SDA and SCL Lines
- Prevents SDA and SCL Corruption During Live Card Insertion and Removal from Backplane
- Ability to Isolate Input SDA and SCL Lines from Output

- Compatible with I²C™, I²C Fast Mode and SMBus Standards
- Small MSOP 8-Pin Package
- dV/dt Rise Time Accelerators on All SDA and SCL Lines
- Low I_{CC} Chip Disable: <1μA
- READY Open Drain Output
- 1V Pre-Charge on all SDA and SCL Lines

The LTC4300 includes rise time accelerators in combination with weak pull-up resistors meeting both the rise time requirement and low logic level voltage requirement. It is compatible with the I²C, I²C Fast Mode and SMBus Standards. A READY output and ENABLE input allow the user to hot swap the card yet keep it isolated until it is needed.

The LTC4300 is available in the MSOP 8-pin package taking up very little space. ■

Load Share Controller Eliminates "OR"ing Diodes for N+1 Redundant Supplies

Linear Technology introduces the LTC4350, a controller that allows the load current to be equally shared among multiple power supplies. By using isolation FETs

and very low value sense resistors, it provides over-voltage, under-voltage and reverse current protection without the losses associated with "OR"ing diodes. The LTC4350 isolates the power supply from output failures, provides a status indicator and allows the power supply to be hot swapped without turning off system power. The part communicates with other devices through a share bus and adjusts the power supply voltage to assure equal load sharing among all the power supplies in high

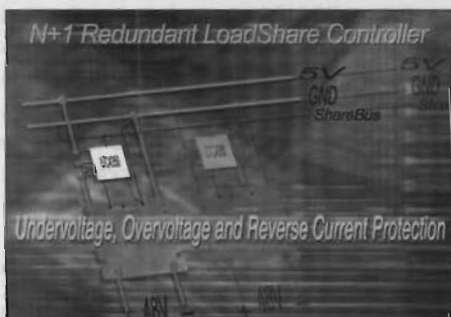


FIGURE 1. LTC4350 SIMPLIFIES LOAD SHARING BETWEEN MODULES

Summary of Features:

- Load Share Control for N+1 Redundant Supplies
- Allows Power Supply to Be Hot Swapped
- Isolates Supply Failures from Output
- Eliminates "OR"ing Diodes
- Identifies and Localizes Output Low, Output High and Open-Circuit Faults
- Controls Output Voltages from 1.5V to 12V

power and high reliability systems such as network servers, telecom and base station equipment or other distributed power supply applications. ■

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Ramp Three Supplies with a Supply Monitor and Hot Swap Controller

Many multiply supplied digital systems require simultaneous ramping of supplies at power up. Since the power supply usually consists of separate regulators for each voltage, it is impossible to guarantee simultaneity of output. The circuit shown in Figure 1 ramps the outputs of three supplies and ensures tracking at power up and during recovery from a fault.

Regulators invariably start up at different rates and different times based on current capability, filter capacitance and loop characteristics, so there are no guarantees as to how or when the outputs will rise to their respective voltages. In this case, an LTC1728-2.5 triple supply monitor keeps watch over each of three regulated supplies (1.8V, 2.5V and 3.3V). When all supplies rise to within acceptable limits (typically within 7.5% of the nominal output voltage), the LTC1728 waits 200ms and then enables an LTC1422 Hot Swap™ controller. The LTC1422 introduces an additional delay of approximately 1.4 seconds and then ramps the gates of

FIGURE 1. RAMPING THREE SUPPLIES

three N-channel MOSFETs, one in series with the output of each supply. Figure 2 shows the relative timing of various waveforms during start-up.

Arranged as source followers, the MOSFETs nominally track as the LTC1422 ramps a common gate node. The ramp rate is set by the GATE pin current and capacitor C_G according to the equation where I_{GATE} is typically 17μA and C_G is selected to limit the rate of rise and therefore the

inrush current into any subsequent load capacitance.

The highest output, 3.3V, is the last to reach its final voltage. Its condition is monitored by the LTC1422's FB pin, which releases RESET when the 3.3V MOSFET is fully on. RESET

goes high after 1.4 second delay and, in turn, initiates load activity.

Faults

Output faults are handled by the short-circuit limiting of each individual DC/DC converter. Nevertheless, if a fault does occur, the effects are short lived. If one of the regulators goes into current limiting, its output will fall and the LTC1728's RST output will go low. The LTC1422 then shuts off all of the outputs. This effectively removes the fault from the output of the affected regulator. The regulator output recovers and, after delays of 200ms and 1.4s, the LTC1422 tries to bring up the load again. If the fault persists, the regulator output will droop and the cycle repeats. Diodes are included across the outputs to guarantee worst-case differential levels under catastrophic fault conditions. Note that to compensate for MOSFET drops, the regulators are adjusted approximately 100mV higher than nominal. ■

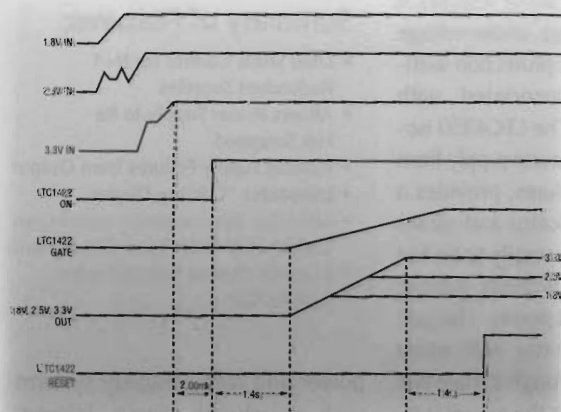
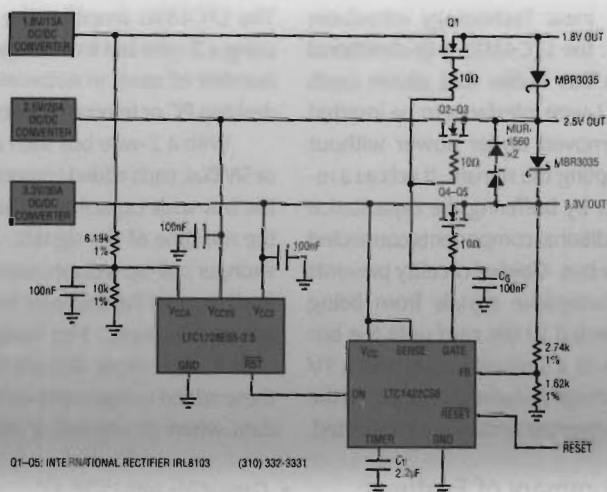


FIGURE 2. TIMING DIAGRAM



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